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Application for Letters Patent

Title   :   NONVOLATILE SEMICONDUCTOR STORAGE DEVICE

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NONVOLATILE SEMICONDUCTOR STORAGE DEVICE

RELATED APPLICATION DATA

The present application claims priority to Japanese Application P2000-110139 filed April 12, 2000, which

5   application is incorporated herein by reference to the extent permitted by law.

BACKGROUND OF INVENTION

Field of the Invention

This invention relates to a nonvolatile semiconductor

10   storage device, and more particularly, to a nonvolatile semiconductor storage device using a ferroelectric thin film.

Description of the Related Art

Various proposals and suggestions regarding the

15   construction of nonvolatile semiconductor storage devices of high integration density in terms of use of ferroelectric thin films for semiconductor storage elements are known. In the currently available technology for designing or fabricating such nonvolatile storage devices, the quantity

20   of change in the residual spontaneous polarization of the ferroelectric thin film within the operational guaranteed temperature of the coercive electric field serves as one of the criteria in determining design margin.

However, the existing method of securing the design

25   margin entails a drawback well known to those active in the field, in that restraint of the freedom of device design is created, standing as an obstacle to the realization of storage devices of high integration.

SUMMARY OF THE INVENTION

30   It is therefore an object of the present invention

to provide a nonvolatile semiconductor storage device of high integration density which can resolve the aforementioned disadvantage.

A nonvolatile semiconductor storage device according to the present invention comprises a nonvolatile semiconductor storage device provided with a capacitor using a ferroelectric thin film, wherein an apparent coercive electric field value in the operational guaranteed temperature range of the nonvolatile semiconductor storage device when regarded as the voltage applied to the capacitor remains within the range of design margin of the nonvolatile semiconductor storage device in the coercive electric field value at the specified temperature.

For example, when regarded in terms of the voltage applied to the aforementioned capacitor, the rate of change in the temperature of the apparent coercive electric field is 0.3%/°C or lower in the operational guaranteed temperature range of the nonvolatile semiconductor storage device. Also, the design margin associated with the coercive electric field is lowered by constructing a complex capacitor structure for the capacitor, wherein a dielectric capacitor with a dielectric thin film having such a temperature dependency that the dielectric constant thereof decreases accompanying an increase in temperature over the operational guaranteed temperature range of the nonvolatile semiconductor storage device mentioned above is serially connected with a dielectric capacitor provided with a ferroelectric thin film.

In the nonvolatile semiconductor storage device

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mentioned above, changes of the coercive electric field in the operational guaranteed temperature are kept down to a minimum, so that the design margin of a nonvolatile storage device element becomes small, thus realizing a

5 ferroelectric, nonvolatile storage device of high integration density.

The coercive electric field of a ferroelectric typically decreases in proportion to the power of 1.5 of (T-Tc), where T denotes the sample temperature T and Tc

10 denotes the ferroelectric phase transition temperature. Consequently, for instance, assume that the change of the coercive electric field accompanying a temperature increase from the room temperature to 80°C needs to be suppressed to 10% or less. Then, it would be necessary

15 for Tc to exceed approx. 800°C. This means that the selection of materials for a ferroelectric thin film is likely to turn out substances such as $LiNbO_3$ (Tc=1483K), and $La_2Ti_2O_7$ (Tc=1773K), $Nd_2Ti_2O_7$ (Tc=1773K), and $Sr_2Nb_2O_7$ (Tc=1615K) which have a structure of $Sr_2Nb_2O_7$, and Bi_2WO_6

20 (Tc=1208K), Bi_3TiNbO_9 (TC=1213K), and Bi_3TiTaO_9 (Tc=1143K) which have a layer structure.

Moreover, in the above mentioned nonvolatile semiconductor storage device, the design margin associated with the coercive electric field decreases

25 through construction of a complex capacitor structure for the capacitor, thereby resulting in diminishing the design margin of a nonvolatile storage element using a ferroelectric and realizing a ferroelectric nonvolatile storage device of high integration density.

30 The above-mentioned complex capacitor is, for example, a ferroelectric capacitor serially connected

with a capacitor (compensation capacitor) using a
dielectric thin film having such a temperature dependency
that the dielectric constant thereof tends to decrease
accompanying the increase in the temperature of a

5   material. In such a complex capacitor, compensation for
the temperature dependency of the coercive electric field
is performed by reducing the voltage to be applied to the
ferroelectric capacitor accompanying the increase in the
capacitor temperature.

10   For materials of the compensation capacitor which
can compensate for the temperature dependency of the
coercive electric field, there are available, for
instance, $Pb(M_{1/3}Nb_{2/3})O_3$ (where M=Co, Ni, Mg),
$Pb(M_{1/3}Ta_{2/3})O_3$ (where M=Co, Ni, Mg), and $Pb(Fe_{2/3}W_{1/3})O_3$,

15   wherein position B of a ferroelectric having the
Perovskite structure (ABO_3) is composed of a mixture of
two kinds of elements. In these materials, a phase
change from normal dielectric phase to ferroelectric
phase occurs in the vicinity of 180K to 80K, which is

20   sufficiently lower than the operational guaranteed
temperature of a device (*e.g.*, -40°C), at which they have
no spontaneous polarization, showing characteristics as
the dielectrics of high dielectric constants.

Further, voltage applied to the complex capacitor is
25   distributed to the ferroelectric capacitor and the
compensation capacitor. The voltage thus distributed to
the compensation capacitor is determined in terms of a
balance between the effective performance of compensation
and suppression of the operating voltage of the device as

30   a result of distribution of no excessive.

Take, for instance, a case of using an SBT thin film

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for the ferroelectric capacitor. If the compensation capacitor should take the same shape as that of the ferroelectric capacitor, a dielectric constant of about 500 or more is necessary for the voltage associated with

5   the compensation capacitor to be about 0.5 times that of the SBT. Also, in a case of using a PZT film for the ferroelectric capacitor, it is desirable to use a substance of even higher dielectric constant for the thin film material of the compensation capacitor.

10   As the foregoing explanation shows, the present invention provides a nonvolatile semiconductor storage device in which the design margin associated with the coercive electric field of the nonvolatile semiconductor storage device can be reduced by keeping any change in

15   the operational guaranteed temperature of the coercive electric field down to a minimum. Inasmuch as this reduction makes it possible to diminish the design margin of a nonvolatile semiconductor storage device of high integration density, a ferroelectric nonvolatile

20   semiconductor storage device subjected to a more rigorous criterion of design margin, namely, a ferroelectric nonvolatile storage device of high integration density, can be realized.

        Other objects and features of the present invention

25   will appear in the course of the description thereof which follows.

        BRIEF DESCRIPTION OF THE DRAWINGS

        FIG. 1 shows schematically a section of a first

30   preferred embodiment of a nonvolatile semiconductor storage device according to the present invention;

FIGs. 2A to 2E are cross-sectional views of a fabrication process illustrating a fabrication method of a nonvolatile semiconductor storage device described in a first preferred embodiment;

5   FIG. 3 shows schematically a section of a second preferred embodiment of a nonvolatile semiconductor storage device according to the present invention;

FIGs. 4A to 4E are cross-sectional views of a fabrication process illustrating a fabrication method of

10   a nonvolatile semiconductor storage device described in a second preferred embodiment;

FIG. 5 shows schematically a section of a third preferred embodiment of a nonvolatile semiconductor storage device according to this invention;

15   FIGs. 6A to 6D are cross-sectional views of a fabrication process illustrating a fabrication method of a nonvolatile semiconductor storage device described in a third preferred embodiment.

20   DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of this invention will now be described with reference to the accompanying drawings. Through proper selection of the material for the ferroelectric thin film so as to minimize changes in the

25   operational guaranteed temperature of the coercive electric field, the design margin of the nonvolatile storage element using the ferroelectric thin film is made small to materialize the ferroelectric nonvolatile storage device of high integration density.

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First Embodiment

A nonvolatile semiconductor storage device according to a first embodiment of the present invention will now be explained with reference to a schematic cross-sectional view of Fig. 1.

5   As shown in Fig. 1, an element isolation oxide film 12 separating an element forming region is formed on a semiconductor substrate 11 (*e.g.*, p-type silicon substrate). On the element forming region of the semiconductor substrate 11 is formed a gate insulating

10   film 13 comprising a silicon oxide film of 1.5nm thick, for example, and a silicon nitride film of 2 nm thick, for example.

On the above-mentioned gate insulating film 13 is formed a gate electrode 14. Further, a source region 15

15   is formed on one side of the gate electrode 14 on the semiconductor substrate 11, while a drain region 16 is formed on the other side thereof on the semiconductor substrate 11. A transistor Tr is constructed in this manner.

20   On the substrate 11, a first interlayer insulating film 17 covering the transistor Tr is deposited and formed, for instance, by depositing the silicon oxide film of 700nm thick. In this first interlayer insulating film 17 are formed a contact hole 18 extending to the

25   drain region 16 and a connection pattern groove 19 stretching out continuously to the contact hole 18, in which a plug 20 comprised of polysilicon is formed, while inside the connection pattern groove 19 is formed a conductive pattern 21 composed of polysilicon. As shown

30   in the figure, a silicide layer 41 may be formed on top of the conductive pattern 21.

On the first interlayer insulating film 17 is formed
a barrier layer 22 connecting with the conductive pattern
21. This barrier layer 22 comprises, as an example, a
titanium (Ti) film fully grown to a thickness of 20nm and
5   a titanium nitride (TiN) thin film fully grown to a
thickness of 50nm thereon.

On the barrier layer 22 is formed a lower electrode
31 comprising a platinum thin film of 200nm thick, for
example. Also, on the lower electrode 31 is formed a
10 ferroelectric thin film 24 comprising a Bi_3TiTaO_9 thin
film having a thickness of 80nm to 120nm, for example.
Furthermore, on the ferroelectric thin film 24 is formed
an upper electrode 32 comprising a platinum thin film.
As described above, the capacitor 30 is comprised of the
15 lower electrode 31, the ferroelectric thin film 24, and
the upper electrode 32.

Insofar as the ferroelectric thin film 24 is a
metal oxide having a layer structure or a metal oxide
having an $Sr_2Nb_2O_7$ structure as the metallic oxide with
20 the phase transition point from ferroelectric to normal
dielectric of 800°C or higher, it is not limited to
Bi_3TiTaO_9.

Moreover, a second interlayer insulating film 35 is
formed through deposition of a silicon oxide film with a
25 thickness of 200nm, for example, in the manner of
covering the aforementioned capacitor 30. On this second
interlayer insulating film 35 is formed a connection
aperture 36 extending to the upper electrode 32, and a
wiring 37 connecting with the upper electrode 32 via the
30 connection aperture 36 is formed on the second interlayer
insulating film 35, a protective film 38 covering the

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wiring 37 being further formed thereon with a pad (not shown) formed on the protective film 38.

Normally, the coercive electric field of a ferroelectric decreases in proportion to the power of 1.5 of (T-Tc), where the sample temperature is T and the ferroelectric phase transition temperature is Tc. Consequently, suppose that the change of the coercive electric field accompanying a temperature increase from the room temperature to 80°C is to be suppressed to 10% or less. Then Tc needs to be approx. 800°C or higher. This means that the selection of materials for a ferroelectric thin film would present candidates such as $LiNbO_3$ (Tc=1483K), and $La_2Ti_2O_7$ (Tc=1773K), $Nd_2Ti_2O_7$ (Tc=1773K), and $Sr_2Nb_2O_7$ (Tc=1615K) which have a structure of $Sr_2Nb_2O_7$, and Bi_2WO_6 (Tc=1208K), Bi_3TiNbO_9 (TC=1213K), and Bi_3TiTaO_9 (Tc=1143K) which have a layer structure.

In addition, when such factors as the rate of change in the temperature of the apparent coercive electric field to be 0.3%/°C or less in the operational guaranteed temperature range of the nonvolatile semiconductor storage device, the ease of crystallization, and the possibility of obtaining large spontaneous polarization are all taken into consideration, it is preferable to use Bi_3TiNbO_9 or Bi_3TiTaO_9 as the ferroelectric material of a capacitor.

Hence, in the nonvolatile semiconductor storage device of the foregoing first preferred embodiment, Bi_3TiTaO_9 is used as the ferroelectric material of the capacitor. Any change in the coercive electric field accompanying an increase in the temperature of the ferroelectric (an increase from the room temperature of

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25°C to 80°C, for example) can thus be suppressed to 10% or less. Accordingly, the design margin of a nonvolatile storage device becomes small, thus making it possible to bring about a ferroelectric, nonvolatile storage device

5   of high integration density.

Now referring to sectional views of the fabrication process from Figs. 2A to 2E, a method of fabricating the nonvolatile semiconductor storage device described in the preceding first preferred embodiment will be explained.

10   As Fig. 2A shows, after the element isolation oxide film 12 is formed on the semiconductor substrate 11 (for example, p-type silicon substrate) by the selective oxidation process, the semiconductor substrate 11 is heated to 800°C and subjected to exposure to oxygen gas

15   diluted with nitrogen gas, a silicon oxide film of 1.5nm thick, for example, is formed on the exposed surface of the semiconductor substrate 11. Further processing by reduced pressure CVD forms a silicon nitride of 2nm thick, for example, to be used as the gate insulation film 13.

20   The subsequent step includes the formation of an electrode forming film by producing a gate electrode thin film and a titanium nitride thin film. This is followed by forming a photoresist film (not shown) by the coating technique, whereafter the photoresist film is subjected

25   to patterning into the shape of a gate electrode pattern by the lithographic process (exposure, development, baking, etc.), the patterned photoresist film being next employed as a mask for etching the electrode forming film to form the gate electrode 14. Further, impurity (*e.g.*,

30   arsenic) is introduced into the semiconductor substrate 11 by ion implantation using the photoresist film and the

element isolation oxide film 12 as the masks to form the source region 15 and the drain region 16. The photoresist film is then stripped.

The succeeding step entails the formation of the

5   first interlayer insulation film 17 through the deposition step of a silicon oxide film of 700nm thick, for example, on the semiconductor substrate 11 by CVD, while the substrate temperature at the time of film making for the first interlayer insulation film 17 was

10   set at 400°C, for example. This is followed by the step of forming the contact hole 18 which exposes the drain region 16 and the connection pattern groove 19 which stretches out continuously to the contact hole 18.

Then, after polysilicon is deposited with a

15   thickness of 600nm, for example, in the manner of embedding it inside the contact hole 18 and the connection pattern groove 19, it is subjected to the heat treatment in nitrogen at 850°C for 30 minutes, for example. Thereafter, an excess polysilicon film on the

20   first interlayer insulating film 17 is removed, *e.g.*, by CMP (Chemical Mechanical Polishing) to produce the plug 20 inside the contact hole 18 as well as the conductive pattern 21 inside the connection pattern groove 19. Note that, as shown in the figure, to improve the conductivity

25   of the conductive pattern 21, silicide processing may be applied to the top of the conductive pattern 21 to form the silicide layer 41.

The subsequent step includes rinsing of the semiconductor substrate 11, which is then heated or

30   exposed to an atmosphere under reduced pressure for dehydration, whereupon a process such as sputtering takes

over to produce a titanium (Ti) thin film (not shown) of 20nm thick, for example, then a titanium nitride (TiN) thin film of 50nm thick, for example, thereby forming the barrier layer 22. Next, a lower electrode thin film 23 comprised of a platinum (Pt) film is produced with a thickness of 200nm, for example.

As an example of the foregoing film making conditions of each film, the substrate temperature may be set at 200°C, for example, when making a titanium (Ti) thin film, 25°C, for example, when making a titanium nitride (TiN) thin film, or 400°C, for example, when making a platinum thin film. The pressure of film-making atmosphere in any of these cases may be set at 0.53Pa with DC power at 2kW. Each of the above-mentioned films is heat-treated for 1 hour in a nitrogen atmosphere of 400°C to 700°C, as necessary, to form the stable lower electrode thin film 23.

As shown in Fig. 2B, the rotary coating method follows to make a Bi_3TiTaO_9 precursor thin film. First, the elements of Bi, Ti, and Nb are compared to the stoichiometric composition of Bi_3TiTaO_9, and on the aforementioned semiconductor substrate 11 which was subjected to all the processing steps up to and including the formation of the lower electrode thin film 23 thereon, a series of processing steps of coating a solution of organic metals containing a 1% to 1.5% excess of Bi, drying, and rapid thermal annealing (RTA) are performed one time or several times, whereupon, as necessary, an oxidation processing using ozone is performed at lower temperatures under 500°C to form a precursor (oxide) thin film.

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The precursor (oxide) thin film next undergoes the crystallization process in an oxidative or neutral atmosphere at the specified temperature between 500°C and 750°C, thereby forming a ferroelectric thin film 24

5   comprising a Bi_3TiTaO_9 thin film of a thickness of 80nm to 120nm the lower electrode thin film.

Insofar as the ferroelectric thin film 24 is a metallic oxide having a layer structure or an $Sr_2Nb_2O_7$ structure as the metallic oxide with its phase transition

10 point from ferroelectric to normal dielectric of over 800°C, it is not limited to Bi_3TiNbO_9.

Subsequently, the upper electrode thin film 25 comprised of a platinum thin film mentioned above is formed on the ferroelectric thin film 24 by sputtering.

15 As an example of the film-making conditions of this platinum thin film, the following settings may be used: the specified temperature between 25°C and 400°C for the substrate temperature, 0.53Pa for the pressure of film-making atmosphere, and 2kW for DC power. The heat

20 treatment may be performed, as necessary, in a nitrogen atmosphere at 550°C to 700°C or in a mixed atmosphere of oxygen and nitrogen for 30 minutes to 1 hour, thereby improving the crystallinity of the ferroelectric thin film 24 and the upper electrode thin film 25.

25 As shown in Fig. 2C, after the formation of a photoresist film (not shown) by the coating technique on the upper electrode thin film 25, the photoresist film is patterned by the lithographic process (exposure, development, baking, etc.) into the shape of a capacitor

30 pattern. Then, the patterned photoresist film is used as a mask for etching from the upper electrode thin film 25

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to the barrier layer 22 so as to form the capacitor 30
comprising the lower electrode 31 comprised of the lower
electrode thin film 23 and the upper electrode 32
comprised of the ferroelectric thin film 24 and the upper
5   electrode thin film 25. The photoresist film is then
removed.

It should be pointed out that a hard mask may be
used instead of the photoresist film. After the removal
of the mask film, as necessary, the heat treatment may be
10   performed in nitrogen atmosphere or a mixed atmosphere of
oxygen and nitrogen at 550°C to 700°C for 30 minutes to 1
hour, thereby improving the crystallinity of the
ferroelectric thin film 24.

Referring next to the drawing in Fig. 2D, a silicon
15   oxide film is deposited by CVD with a thickness of 200nm,
for example, in the manner of covering the capacitor 30,
forming the second interlayer insulating film 35 on the
first interlayer insulating film 17. The substrate
temperature when making film for the second interlayer
20   insulating film 35 was set at 400°C, for example.

Thereafter, after a photoresist film (not shown) is
formed by the coating technique on the second interlayer
insulating film 35, an opening pattern to form a
connection aperture extending to the upper electrode 32
25   of the capacitor 30 is formed by the lithographic process
(exposure, development, baking, etc.), followed by a dry
etching process of the second interlayer insulating film
35 using the patterned photoresist film as a mask for
forming the connection aperture 36 extending to the upper
30   electrode 32. The photoresist film is then stripped.

As illustrated in Fig. 2E, after a wiring metal film

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is formed on the second interlayer insulating film 35 in
the manner of embedding the preceding connection aperture
36 by depositing aluminum or aluminum alloy, for example,
the wiring metal film is subjected to patterning to form
5   the wiring 37 connecting the connection aperture 36 with
the upper electrode 32.

The protective film 38 covering the wiring 37 on the
second interlayer insulating film 35 is next formed of
such an insulating film containing a silicon nitride film,
10   and there follows a step, not illustrated, of coating a
photoresist, which is subjected to patterning by the
lithographic process (exposure, development, baking,
etc.) in the shape of a pad to take out wiring, whereupon
this photoresist pattern is used as the mask to perform
15   dry etching of the protective film 38, thus forming the
pad (not shown).

Second Embodiment

Now, referring to a schematic cross-sectional
20   view of Fig. 3, a modified nonvolatile semiconductor
storage device according to a second embodiment will be
described with an explanation of a nonvolatile
semiconductor storage device using Bi_3TiNbO_9 as the
ferroelectric material of a capacitor.

25   As shown in Fig. 3, an element isolation oxide film
12 separating an element forming region is formed on a
semiconductor substrate 11 (e.g., p-type silicon
substrate). In the element forming region of the
semiconductor substrate 11 is formed a gate insulating
30   film 13 comprising a silicon oxide film of a thickness of
1.5nm, for example, and a silicon nitride film of a

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thickness of 2nm, for example.

A gate electrode 14 is formed on the gate insulating film 13. In addition, a source region 15 is formed on one side of a gate electrode 14 on the semiconductor substrate 11, while a drain region 16 is formed on the other side thereof on the semiconductor substrate 11. A transistor Tr is constructed in this manner.

On the semiconductor substrate 11 is formed a first interlayer insulating film 17 covering the transistor Tr through the steps of deposition and formation of, for example, a silicon oxide film of a thickness of 700nm, for example. On this first interlayer insulating film 17 is formed the contact hole 18 extending to the drain region 16. A plug 20 composed of polysilicon is formed inside the contact hole 18. As shown in the figure, a silicide layer 41 may be formed on top of the plug 20.

On the semiconductor substrate 11 is formed a barrier layer 22 connecting with the plug 20, the barrier layer 22 comprising, as an example, a titanium nitride film grown to a thickness of 20nm and an iridium (Ir) thin film grown to a thickness of 50nm thereon. In addition, on the barrier layer 22 is formed the lower electrode 31 comprising the platinum (Pt) thin film of a thickness of, e.g., 200nm.

A ferroelectric thin film 24 comprising, for example, a Bi_3TiNbO_9 thin film of a thickness of 80nm to 120nm is formed on the lower electrode 31. Insofar as the ferroelectric thin film 24 is a metal oxide having a layer structure or a metal oxide having an $Sr_2Nb_2O_7$ structure as the metal oxide with its phase transition point from ferroelectric to normal dielectric of 800°C or

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higher, it is not limited to Bi_3TiNbO_9.

Further, on the ferroelectric thin film 24 is formed an upper electrode thin film 25 comprising the iridium thin film. As described above, a capacitor 30 comprises the lower electrode 31, the ferroelectric thin film 24, and an upper electrode 32.

Still further, a second interlayer insulating film 35 is formed through the deposition of a silicon oxide film with a thickness of, *e.g.*, 200nm, in the manner of covering the capacitor 30. On this second interlayer insulating film 35 is formed the connection aperture 36 extending to the upper electrode 32. On the second interlayer insulating film 35 is formed a wiring 37 made of, *e.g.*, aluminum or aluminum alloy, connecting with the upper electrode 32 via the connection aperture 36. On the interlayer insulating film 35 is formed a protective film 38 which covers the wiring 37, and the pad (not shown) is formed on the protective film 38.

Accordingly, in the nonvolatile semiconductor storage device according to the second embodiment, Bi_3TiNbO_9 is used as the ferroelectric substance of the capacitor material, so that any change in the coercive electric field accompanying a temperature increase of the ferroelectric material (e.g., from the room temperature of 25°C to 80°C) may be suppressed to under 10%, thus reducing the design margin of the nonvolatile semiconductor storage device and realizing a ferroelectric nonvolatile storage device of high integration density.

Next, a method of fabricating the nonvolatile semiconductor storage device which was explained in the

aforementioned second embodiment will be described with reference to the cross-sectional views of the fabrication process from Fig. 4A to Fig. 4E.

As Fig. 4A shows, after the element isolation oxide
5 film 12 is formed on the semiconductor substrate 11 (*e.g.,* p-type silicon substrate) by the selective oxidation process, the semiconductor substrate 11 is heated to 800°C and subjected to exposure to oxygen gas diluted with nitrogen gas, a silicon oxide film of 1.5nm thick,
10 for example, is formed on the exposed surface of the semiconductor substrate 11. Further processing by reduced pressure CVD forms a silicon nitride film of 2nm thick, for example, which serves as the gate insulating film 13.

15 After the next step of forming an electrode forming film by producing a gate electrode thin film and a titanium nitride thin film, a photoresist film (not shown) is formed by the coating technique, whereupon the photoresist film is subjected to patterning into the
20 shape of a gate electrode pattern by the lithographic process (exposure, development, baking, etc.). Then, the patterned photoresist film is used as a mask for etching the electrode forming film to form the gate electrode 14. The next step is an introduction of impurity (*e.g.,*
25 arsenic) into the semiconductor substrate 11 by ion implantation using the photoresist film and the element isolation oxide film 12 as the masks to form the source region 15 and the drain region 16. After this process comes the stripping of the photoresist film.
30 The succeeding step involves the use of CVD to form the first interlayer insulating film 17 through the

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deposition of a silicon oxide film of 700nm thick, for
example, on the semiconductor substrate 11. The
substrate temperature in film making for the first
interlayer insulating film 17 is set at 400°C, for
5   example. Thereafter, the formation of the contact hole
18 which exposes the drain region 16 follows.

In addition, after the deposition step of
polysilicon with a thickness of 600nm, for example, in
the manner of embedding it inside the contact hole 18, it
10   is subjected to the heat treatment in nitrogen at 850°C
for 30 minutes, for example. Then, an excess polysilicon
film on the first interlayer insulating film 17 is
removed by CMP (Chemical Mechanical Polishing) to produce
the plug 20 inside the contact hole 18, for example. It
15   should be noted that to improve the conductivity of the
plug 20, silicide processing may be applied on an upper
surface of the plug 20 for the formation of the silicide
layer 41.

This is succeeded by the rinsing step of the
20   semiconductor substrate 11 which is then heated or
exposed to a reduced pressure atmosphere for dehydration.
Then, a processing step such as sputtering takes over to
produce a titanium (Ti) thin film of 20nm thick, for
example, then an iridium (Ir) thin film of 50nm thick,
25   for example, thereby forming the barrier layer 22. Next,
the lower electrode thin film 23 comprised of a platinum
(Pt) thin film is produced with a thickness of, *e.g.*,
200nm.

As an example of the foregoing film-forming
30   conditions of each film, the substrate temperature may be
set at 25°C, for example, when making a titanium nitride

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(TiN) thin film, 400°C, for example, when making an
iridium (Ir) thin film 22, or 400°C, for example, when
making a platinum (Pt) thin film 23, the pressure of
film-making atmosphere in any of these cases being set at
5   0.53Pa with DC power at 2kW, while each of the
aforementioned thin films is heat-treated for one hour in
a mixed atmosphere of oxygen and nitrogen at 400°C to
700°C, as necessary, to form the stable lower electrode
thin film 23.
10   As shown in Fig. 4B, the rotary coating method
follows to make a Bi_3TiNbO_9 precursor thin film. First,
the elements of Bi, Ti, and Nb are compared to the
stoichiometric composition of Bi_3TiNbO_9; and on the
semiconductor substrate 11 which underwent all the steps
15 up to and including the formation of the lower electrode
thin film 23, a series of processing steps of coating a
solution of organic metals containing a 1% to 1.5% excess
of Bi, drying, and rapid thermal annealing (RTA) are
performed one time or several times, and, as necessary,
20 oxidation processing using ozone is conducted at low
temperatures 500°C or lower to form a precursor (oxide)
thin film. The precursor (oxide) thin film is then
processed with oxidation in an oxidative or neutral
atmosphere at the specified temperature between 500°C and
25 750°C, resulting in the formation of a ferroelectric thin
film 24 comprising a Bi_3TiNbO_9 thin film of a thickness
of 80nm to 120nm thereon.
      Insofar as the ferroelectric thin film 24 is a metal
oxide having a layer structure or a $Sr_2Nb_2O_7$ structure as
30 the metallic oxide with its phase transition point from
ferroelectric to normal dielectric of 800°C or higher, it

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is not limited to Bi_3TiNbO_9.

Subsequently, the upper electrode thin film 25 comprised of an iridium thin film is formed on the ferroelectric thin film 24 by sputtering. As an example of film-making conditions of this iridium thin film, the specified temperature between 25°C and 400°C may be set for the substrate temperature with 0.53Pa for the pressure of film-making argon atmosphere and 2kW for DC power, for example. The heat treatment may be performed, as necessary, in nitrogen atmosphere or a mixed atmosphere of oxygen and nitrogen at 550°C to 700°C for 30 minutes to 1 hour, thereby improving the crystallinity of the ferroelectric thin film 24 and the iridium thin film.

As illustrated in Fig. 4C, after the formation of a photoresist film (not shown) by the coating technique on the upper electrode thin film 25 comprised of the iridium thin film, the photoresist film is patterned by the lithographic process (exposure, development, baking, etc.) into the shape of a capacitor pattern. Then, the patterned photoresist film is used as a mask for etching from the aforementioned upper electrode thin film 25 to the barrier layer 22, thus forming a capacitor 30 comprising the lower electrode 31 which is comprised of the lower electrode thin film 23 and the upper electrode 32 which is comprised of the ferroelectric thin film 24 and the upper electrode thin film 25. The process of stripping the photoresist film follows.

It should be pointed out that a hard mask may be used instead of the photoresist film. After the removal of the mask film, as necessary, the heat treatment may be

conducted in nitrogen atmosphere or a mixed atmosphere of oxygen and nitrogen at 550°C to 700°C for 30 minutes to 1 hour with a resultant improvement of the crystallinity of the ferroelectric thin film 24.

5   Referring next to Fig. 4D, CVD is used to form the second interlayer insulating film 35 on the first interlayer insulating film 17 through the deposition of a silicon oxide film with a thickness of 200nm, for example, in the manner of covering the aforementioned capacitor 30.

10   The substrate temperature in forming film for the second interlayer insulating film 35 is set at 400°C, for example.

After the subsequent formation of a photoresist film (not shown) by the coating technique on the second

15   interlayer insulating film 35, an opening pattern to form a connection aperture extending to the upper electrode 32 of the capacitor 30 is formed by the lithographic process (exposure, development, baking, etc.), followed by a dry etching process of the interlayer insulating film 35 with

20   the patterned photoresist film as the mask to form a connection aperture 36 which extends to the upper electrode 32. The stripping of the photoresist film follows.

As illustrated in Fig. 4E, after a wiring metal film

25   is formed on the second interlayer insulating film 35 in the manner of embedding the connection aperture 36 by depositing aluminum or aluminum alloy, for example, the wiring metal film is subjected to patterning to form the wiring 37 connecting the connection aperture 36 with the

30   upper electrode 32.

The protective film 38 covering the wiring 37 on the

second interlayer insulating film 35 is next formed of such an insulating film containing a silicon nitride film. There follows a step, not illustrated, of coating a photoresist, which is subjected to patterning by the

5   lithographic process (exposure, development, baking, etc.) in the shape of a pad to take out wiring, whereupon this photoresist pattern is used as the mask to perform dry etching of the protective film 38, thus forming the pad (not shown).

10   In the nonvolatile semiconductor storage device, the use of a complex capacitor structure designed to minimize any change of the coercive electric field in the operational guaranteed temperature contributes to reducing the design margin of a nonvolatile storage

15   element of high integration density, thus realizing a ferroelectric, nonvolatile storage device of high integration density.

Third Embodiment

20   Now, referring to a schematic section of Fig. 5, another modified nonvolatile semiconductor storage device according to a third embodiment will be described with an explanation of a nonvolatile semiconductor storage device employing a complex capacitor structure.

25   As depicted in Fig. 5, an element isolation oxide film 12 separating the element forming region is formed on a semiconductor substrate 11 (e.g., p-type silicon substrate). In the element forming region of the semiconductor substrate 11 is formed a gate insulating

30   film 13 comprised of a silicon oxide film of 1.5nm thick, for example, and a silicon nitride film of 2nm thick, for

example.

A gate electrode 14 is formed on the gate insulating film 13, and a source region 15 is formed on one side of the gate electrode 14 on the semiconductor substrate 11,

5 while a drain region 16 is formed on the other side thereof on the semiconductor substrate 11. A transistor Tr is constructed in this manner.

On the semiconductor substrate 11 is formed a first interlayer insulating film 17 covering the transistor Tr

10 through the deposition and formation of, for example, a silicon oxide film having a thickness of 700nm. A contact hole 18 extending to the drain region 16 and a connection pattern groove 19 stretching out continuously to the contact hole 18 are formed in this first

15 interlayer insulating film 17, a plug 20 comprised of polysilicon being formed inside the contact hole 18 and a conductive pattern 21 comprised of polysilicon being formed inside the connection pattern groove 19. As shown in the figure, a silicide layer 41 may be formed on top

20 of the conductive pattern 21.

On the semiconductor substrate 11, there is formed a barrier layer 22 connecting with the conductive pattern 21. This barrier layer 22 comprises, as an example, a titanium (Ti) film fully grown to a thickness of 20nm

25 with a titanium nitride (TiN) thin film fully grown to a thickness of 50nm formed thereon. In addition, a lower electrode 31 comprised of a platinum thin film having a thickness of 200nm, for example, is formed on the barrier layer 22.

30 On the lower electrode 31, there are formed, sequentially from the bottom layer up, a ferroelectric

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thin film 51 comprising an SBT thin film of a thickness
of 60nm to 120nm, for example, an electrode thin film 52
comprising an iridium thin film, a dielectric thin film
53 comprising a PNN thin film, and an upper electrode 32

5   comprising an iridium thin film. As the foregoing
explanation shows, a complex capacitor 50 is comprised of
the lower electrode 31, the ferroelectric thin film 51,
the dielectric thin film 53, and the upper electrode 32.

     The ferroelectric thin film 51 is available as PZT

10   expressed by $Pb(Zr_xTi_{1-x})O_3$ (where $0.1 \leq x \leq 0.8$), or PZT
added with La or Nb, or PZT part of Pb of which or part
of (Zr, Ti) of which is substituted by Nb. Also, $Sr_{1-x}Bi_{2+x}Ta_2O_9$ (where $0.01 \leq x \leq 0.3$), $Sr_{1-x}Bi_{2+x}Nb_2O_9$ (where $0.01 \leq x \leq 0.3$), and $Sr_{1-x}Bi_{2+x}(Ta_2Nb_y)O_9$ (where $0.01 \leq x \leq 0.3$,

15   $0.1 \leq y \leq 0.5$) are available.

     Certain metals or conductive metal oxides are
available for the electrode thin film 52, for example,
one kind from iridium, platinum, and palladium, or an
alloy or a layer-structure substance composed of at least

20   two kinds of iridium, platinum, and palladium, or
conductive oxides possessing metal conduction such as
iridium oxide (IrO_2), ruthenium strontium oxide ($SrRuO_3$),
and iridium strontium oxide ($SrIrO_3$), or a layer-
structure substance of a metal film and an oxide film.

25   As far as the dielectric thin film 53 is concerned,
it should comprise such a dielectric thin film as to have
a temperature dependency, in which the dielectric
constant decreases accompanying a temperature increase in
the operational guaranteed temperature range of the

30   nonvolatile semiconductor storage device, further
comprising a relaxation type ferroelectric thin film.

For the relaxation type ferroelectric thin film, there
are available such metal oxides as $Pb(M_{1/3}Nb_{2/3})O_3$ (where
$M=Co$, Ni, Mg), $Pb(M_{1/3}Ta_{2/3})O_3$ (where $M=Co$, Ni, Mg), and
$Pb(Fe_{2/3}W_{1/3})O_3$, in which position B of a ferroelectric
5   having the Perovskite structure (ABO_3) comprises a
mixture of two elements.

Moreover, a second interlayer insulating film 35 is
formed through the deposition of a silicon oxide film
with a thickness of 200nm, for example, in the manner of
10   covering the complex capacitor 50. On this second
interlayer insulating film 35 is formed a connection
aperture 36 extending to the upper electrode 32. On the
second interlayer insulating film 35 is formed a wiring
37 made of, for example, aluminum or an aluminum alloy
15   connecting with the upper electrode 32 via the connection
aperture 36. On the interlayer insulating film 35 is
formed a protective film 38 covering the wiring 37, and a
pad (not shown) is formed on the protective film 38.

The capacitor is specially designed in the
20   nonvolatile semiconductor storage device described in
relation to the aforementioned third embodiment, in that
a complex capacitor structure is employed therefor, thus
decreasing the margin of design associated with the
coercive electric field and realizing a ferroelectric
25   nonvolatile storage device of high integration density.

Construction of the complex capacitor is based on,
for example, a ferroelectric capacitor serially connected
with a capacitor (compensation capacitor) using a
dielectric thin film with such a temperature dependency
30   that the dielectric constant thereof tends to decrease
accompanying an increase in the material temperature.

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As the foregoing explanation of the third embodiment shows, connection between the ferroelectric capacitor and the compensation capacitor is so arranged to ensure that the electrode thin film 52 functions as both the

5　electrode of the ferroelectric capacitor and that of the compensation capacitor, while another construction may be used, in which a different conductive material from that of the capacitor electrode is used for connection between the electrode of the ferroelectric capacitor and that of

10　the compensation capacitor.

　　In the complex capacitor, compensation for the temperature dependency of the coercive electric field is rendered by decreasing the voltage to be applied to the ferroelectric capacitor accompanying the increase in the

15　capacitor temperature. For materials of compensation capacitors that can compensate for the temperature dependency of the coercive electric field, there are available, for instance, $Pb(M_{1/3}Nb_{2/3})O_3$ (where M=Co, Ni, Mg), $Pb(M_{1/3}Ta_{2/3})O_3$ (where M=Co, Ni, Mg), and

20　$Pb(Fe_{2/3}W_{1/3})O_3$, wherein a position B of a ferroelectric having the Perovskite structure (ABO_3) is composed of a mixture of two kinds of elements. In these substances, the phase change from normal dielectric phase to ferroelectric phase occurs in the vicinity of 180K to 80K,

25　which is sufficiently lower than the operational guaranteed temperature (e.g., -40°C) of the device, and at the device guaranteed temperature, they have no spontaneous polarization, showing characteristics as the dielectrics of high dielectric constants.

30　　Moreover, the voltage applied to the complex capacitor is distributed to the ferroelectric capacitor

and the compensation capacitor. The voltage thus
distributed to the compensation capacitor is determined
in terms of a balance between the effective performance
of compensation and suppression of the operating voltage
5   of the device through distribution of no excessive
voltage.

Take, for instance, a case of using an SBT thin film
for the ferroelectric capacitor. If the compensation
capacitor should take the same shape as that of the
10   ferroelectric capacitor, a dielectric constant of approx.
500 or more is necessary for the voltage associated with
the compensation capacitor to be about 0.5 times that of
the SBT. Also, suppose that a PZT thin film is employed
for the ferroelectric capacitor. Then, it would be
15   desirable to use a substance having an even higher
dielectric constant for the thin film material of the
compensation capacitor.

When diverse conditions as described above are taken
into consideration, the preferable dielectric substances
20   for the compensation capacitor materials are Pb ($Ni_{1/3}$
$Nb_{2/3})O_3$ and Pb ($Co_{1/3}$ $Nb_{2/3})O_3$.

Moreover, in the aforementioned third preferred
embodiment, although the electrode thin film 52 is formed
between the ferroelectric thin film 51 and the dielectric
25   thin film 53, another acceptable construction may be to
layer the dielectric thin film 53 directly over the
ferroelectric thin film 51 without any formation of the
electrode thin film 52. Such construction including no
electrode thin film 52 means that there is a layer
30   structure of a dielectric thin film (the dielectric thin
film 53) having a temperature dependency, in which the

dielectric constant decreases accompanying the temperature increase in the operational guaranteed temperature range of the nonvolatile semiconductor storage device, and a ferroelectric thin film (the

5   ferroelectric thin film 51) showing a ferroelectric property in the operational guaranteed temperature range, this layered film thus turning into a thin film exhibiting a ferroelectric property. It should be noted that a construction in which the ferroelectric thin film

10   51 is formed at a bottom layer with the dielectric thin film 53 formed on a top layer may be used as well.

Next, a method of fabricating the nonvolatile semiconductor storage device described in the third preferred embodiment will be explained with reference to

15   the sectional views of the fabrication process from Fig. 6A to Fig. 6D.

As Fig. 6A shows, after the element isolation oxide film 12 is formed on the semiconductor substrate 11 (*e.g.*, p-type silicon substrate) by the selective oxidation

20   process, the semiconductor substrate 11 is heated to 800°C and subjected to exposure to oxygen gas diluted with nitrogen gas, a silicon oxide film of 1.5nm thick, for example, is formed on the exposed surface thereof. Furthermore, reduced pressure CVD is used to form a

25   silicon nitride of 2nm thick, for example, for use as the gate insulating film 13.

The succeeding processing step includes the formation of an electrode forming film by producing a gate electrode thin film and a titanium nitride thin film.

30   This is followed by the formation of a photoresist film (not shown) by the coating technique. Then, the

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photoresist film is subjected to patterning into the shape of a gate electrode pattern by the lithographic process (exposure, development, baking, etc.). Next, the patterned photoresist film is put to use as a mask for

5 etching the aforementioned electrode forming film to form the gate electrode 14. Then, impurity (*e.g.*, arsenic) is introduced into the semiconductor substrate 11 by ion implantation using the photoresist film and the element isolation oxide film 12 as the masks to form the source

10 region 15 and the drain region 16. Then the photoresist film is stripped.

Thereafter, a silicon oxide film of 700nm thick, for example, is deposited by CVD on the semiconductor substrate 11 to form the first interlayer insulating film

15 17. The substrate temperature in producing film for the first interlayer insulating film 17 is set at 400°C, for example. This is followed by the formation of the contact hole 18 which exposes the drain region 16 and the connection pattern groove 19 which stretches out

20 continuously to the contact hole 18.

Moreover, after the deposition of polysilicon of a thickness of 600nm, for example, in the manner of embedding it inside the contact hole 18 and the connection pattern groove 19, the heat treatment takes

25 over in nitrogen at 850°C for 30 minutes, for example. Then, an excess polysilicon film on the first interlayer insulating film 17 is removed, *e.g.*, by CMP (Chemical Mechanical Polishing).

The plug 20 is formed inside the contact hole 18 and

30 the conductive pattern 21 is formed inside the connection pattern groove 19 as well. It should be noted that, as

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shown in the figure, to improve the conductivity of the
conductive pattern 21, silicide processing may be applied
to the top of the conductive pattern 21 to form the
silicide layer 41 there.

5   The subsequent step includes rinsing of the
semiconductor substrate 11, which is then heated or
exposed to a reduced pressure atmosphere to perform
dehydration, whereupon a process such as sputtering
succeeds to make a titanium (Ti) thin film (not shown) of
10   20nm thick, for example, then a titanium nitride (TiN)
thin film of 50nm thick, for example, thereby forming the
barrier layer 22. In addition, the lower electrode thin
film 23 comprised of a platinum (Pt) film is made to have
a thickness of 200nm, for example.

15   As an example of the foregoing film making
conditions of each film, the substrate temperature may be
set at 200°C when making a titanium (Ti) thin film, 25°C
when making a titanium nitride (TiN) thin film, or 400°C
when making a platinum thin film, and the pressure of
20   film-making atmosphere in any of these cases may be set
at 0.53Pa with DC power at 2kW. Each of the films
mentioned above is heat-treated for 1 hour in a nitrogen
atmosphere at 400°C to 700°C, as necessary, to form the
stable lower electrode thin film 23.

25   As illustrated in Fig. 6B, the rotary coating method
follows to produce a precursor thin film of SBT, that is,
$Sr_{0.8}Bi_{2.2}Ta_2O_9$ (SBT) having excess of Bi and Sr deficiency.
First, the elements of Sr, Bi, and Ta are compared to the
stoichiometric composition of the SBT. On the
30   aforementioned semiconductor substrate 11 which was
treated with the process of forming a lower electrode

thin film 23 thereon, a series of processing steps of
coating a solution of organic metals containing a 0. 0%
to 5% excess of Bi, drying, and rapid thermal annealing
are performed one time or several times, and, the

5   crystallization process of the formed precursor thin film
in an oxidative or neutral atmosphere is performed at the
specified temperature between 500°C and 750°C, resulting
in the formation of a ferroelectric thin film 51
comprising an SBT thin film of a thickness of 60nm to

10   120nm.

Next, sputtering is applied to form the electrode
thin film 52 comprised of an iridium thin film on the
ferroelectric thin film 51. A good example of film-
making conditions of this iridium thin film includes the

15   specified temperature between 25°C and 400°C for the
substrate temperature, a setting of 0.53Pa argon
atmosphere for film-making atmosphere, and a setting of
2kW for DC power. The heat treatment may be performed,
as necessary, in nitrogen atmosphere or a mixed

20   atmosphere of oxygen and nitrogen at 550°C to 700°C for
30 minutes to 1 hour, thereby improving the crystallinity
of the electrode thin film 52 comprised of the
ferroelectric thin film 51 and the iridium thin film.

The rotary coating method succeeds to produce a

25   precursor thin film of $Pb-(Ni_{1/3}-Nb_{2/3})O_3$ (PNN). First,
the elements of Pb, Ni, and Nb are compared to the
stoichiometric composition of the PNN. On the
aforementioned semiconductor substrate 11 which was
treated with the step of forming the lower electrode thin

30   film 52 thereon, a series of processing steps of coating
a solution of organic metals containing a 3% to 15%

excess of Pb, drying, and rapid thermal annealing (RTA) are performed one time or several times, and, crystallization processing of the formed precursor thin film in an oxidized or neutral atmosphere is conducted at the specified temperature between 500°C and 750°C, resulting in the formation of a ferroelectric thin film 53 comprising a PNN thin film.

Thereafter, sputtering is performed for forming an upper electrode thin film 25 comprising an iridium thin film on the above-mentioned ferroelectric thin film 53. As an example of film-making conditions of this iridium thin film, the specified temperature between 25°C and 400°C may be set for the substrate temperature, 0.53Pa argon atmosphere may be set for film-making atmosphere, and 2kW may be set for DC power. The heat treatment may be conducted, as necessary, in nitrogen atmosphere at 450°C to 700°C for 1 hour, with the result that the crystallinity of the dielectric thin films 51 and 53 (SBT thin film and PNN thin film) and the electrode thin film 52 is improved.

Now, referring to Fig. 6C, after a photoresist film (not shown) is formed on the upper electrode thin film 25 by the coating technique, the photoresist film is subjected to patterning into the shape of a capacitor pattern by the lithographic process (exposure, development, baking, etc.). Next, the patterned photoresist film is employed as a mask for etching from the aforementioned upper electrode thin film 25 to the barrier layer 22 thus to form the complex capacitor comprising the lower electrode 31, which is comprised of the lower electrode thin film 23, and the upper electrode

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32, which is comprised of the ferroelectric thin film 51, the electrode thin film 52, the dielectric thin film 53, and the upper electrode thin film 25. The stripping process of the photoresist film then takes over.

5   It should be noted that a hard mask may be employed instead of the photoresist film. After the removal of the mask film, as necessary, the heat treatment may be conducted in nitrogen atmosphere or a mixed atmosphere of oxygen and nitrogen at 450°C to 700°C for 30 minutes to 1

10   hour, thereby improving the crystallinity of the SBT thin film and the PNN thin film.

Thereafter, CVD is used to form a second interlayer insulating film 35 on the first interlayer insulating film 17 through the deposition of a silicon oxide film of

15   200nm thick, for example, in the manner of covering the complex capacitor 50 mentioned above. The substrate temperature at the time of film making for the second interlayer insulating film 35 is set at, *e.g.*, 400°C, for example.

20   As Fig. 6D shows, a photoresist film (not shown) is next formed by the coating technique on the second interlayer insulating film 35, followed by the process of forming an opening pattern to form a connection aperture extending to the upper electrode 32 of the complex

25   capacitor 50 by means of the lithographic process (exposure, development, baking, etc.). There succeeds the dry etching step of the interlayer insulating film 35 using the patterned photoresist film as the mask to form a connection aperture 36 extending to the upper electrode

30   32. The photoresist film is next removed.

After a wiring metal film is formed on the second

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interlayer insulating film 35 in the manner of embedding
the connection aperture 36 by depositing aluminum or
aluminum alloy, for example, the wiring metal film is
subjected to patterning to form the wiring 37 connecting
5   the connection aperture 36 with the upper electrode 32.

The protective film 38 covering the wiring 37 on the
second interlayer insulating film 35 is next formed of
such an insulating film containing a silicon nitride film.
There follows a step, not illustrated, of coating a
10   photoresist, which is then subjected to patterning by the
lithographic process (exposure, development, baking,
etc.) in the shape of a pad to take out wiring.
Thereafter, this photoresist pattern is used as the mask
to perform dry etching of the protective film 38.   In
15   this manner, the pad (not shown) is formed.

In the aforementioned third embodiment, the
electrode thin film 52 is formed between the
ferroelectric thin film 51 and the dielectric thin film
53.   It should be noted that the dielectric thin film 53
20   may be directly layered on top of the ferroelectric thin
film 51 without undergoing the process of forming the
electrode thin film 52 therebetween.   This arrangement is
tantamount to a lamination of two films, namely, the
dielectric thin film (dielectric thin film 53) having a
25   temperature dependency that decreases accompanying the
temperature increase in the operational guaranteed
temperature range of the nonvolatile semiconductor
storage device and the ferroelectric thin film
(ferroelectric thin film 51) exhibiting a ferroelectric
30   property in the operational guaranteed temperature range,
and thus, this layered film becomes a thin film endowed

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with a ferroelectric property. It should be pointed out
that a reverse arrangement may be put to use, wherein the
bottom layer may be formed of the dielectric thin film 53,
the top layer being formed of the ferroelectric thin film

5   51.

Another advantage of the nonvolatile semiconductor
storage device according to the present invention is the
availability of many choices for materials of thin films.
The following materials may be used for the upper

10 electrode thin film, the lower electrode thin film, the
electrode thin film for capacitor connection, etc.
described in each of the aforementioned preferred
embodiments: one kind of iridium, platinum, or palladium;
an alloy or a layer-structure film composed of at least

15 two kinds of iridium, platinum or palladium; an oxide
conductor showing metallic conduction such as iridium
oxide (IrO_2), ruthenium strontium oxide ($SrRuO_3$), and
iridium strontium oxide ($SrIrO_3$); or a layer-structure
substance comprised of a metal film and an oxide film.

20 The processes for making films of such materials are
feasible if the target quality of the material and the
film-making conditions are modified accordingly. It
should also be noted that the preceding modifications
require corresponding changes in the heat-treatment

25 conditions.

An equally important advantage of the nonvolatile
semiconductor storage device according to the present
invention lies in a fact that the combinations of the
compensation capacitor and the ferroelectric capacitor

30 thin film are not confined to the combinations introduced
to the preferred embodiments mentioned above. For

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instance, the film-making order of the compensation capacitor and the ferroelectric capacitor thin film may be in reverse to that of the foregoing preferred embodiments. This order is determined according to the

5 low or high degree of the heat-treating temperature applied to each film or the drive method of a device.

The scope of the invention is shown by appended claims, and all changes and modifications that fall within the meaning of these claims are contained in this

10 invention.